AMENDMENTS

Please amend the Application, as follows.

In the Claims

Please amend claims 4 and 16, as follows. The "marked-up" version of the amended claim is provided in the APPENDIX attached hereafter.

---

4. (Amended) A liquid crystal display (LCD), comprising:

an LCD panel including:

a first gate line block having a plurality of first gate lines;

a second gate line block having a plurality of second gate lines, said second gate line block formed beneath said first gate line block;

a plurality of first data lines crossing and separated from the first gate lines of said first gate line block;

a plurality of second data lines crossing and separated from the second gate lines of said second gate line block; and

a plurality of pixels formed by areas defined by the gate lines and the data lines, and arrayed in a matrix pattern, the pixels having switching elements coupled to the gate lines and the data lines, and common electrodes to which common voltage is supplied;

a first data driver supplying data voltages, which contain image signals, to the first data lines;

a second data driver supplying data voltages, which contain image signals, to the second data lines;

a first gate driver supplying scanning signals to the gate lines of said first gate line block;

a second gate driver supplying scanning signals to the gate lines of said second gate line block in a scanning direction opposite to that of said first gate driver;

a first frame memory that receives and writes external image signals in synchronization with the write clock signals and outputs the image signals to the first data driver in synchronization with the read clock signals; and

a second frame memory that receives and writes external image signals in synchronization with the write clock signals and outputs the image signals to the second data driver in synchronization with the read clock signals.

16. (Amended) A method for driving a liquid crystal display (LCD) including a first gate line block having a plurality of first gate lines; a second gate line block formed beneath the first gate line block and having a plurality of second gate lines; a plurality of first data lines crossing and separated from the first gate lines of the first gate line block; and a plurality of second data lines crossing and separated from the second gate lines of the second gate line block, comprising the steps of:

providing sequentially scanning signals to the first gate lines of the first gate line block;

providing sequentially scanning signals to the second gate lines of the second gate line block in a scanning direction opposite to that of the first gate line block; and

supplying data voltages, which contain image signals, to the first and second data lines so that the data voltages are supplied to the pixels coupled to the gate lines to which the scanning signals are provided.